Response to Amendment

Applicants' amendment filed on August 09, 2007 has been entered and forwarded to the Examiner on August 16, 2007.

Therefore claims 1 to 21 as recited in the amendment are currently pending in the Application.

Information Disclosure Statement

The Ids filed on Jan. 14, 2005 has been considered and the initialed copy of the PT0-1449 made of record in the file.

Claim Rejections. 35 USC § **102**

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1 to 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshimura et al. (U.S. Patent No. 6,684,007, herein after Yoshimura).

With respect to claim 1 Yoshimura describes a method for etching a solid state material to create a surface relief pattern, the metl~od comprising steps of: forming a photoresist layer on the surface of the solid state material (col. 81 line 39 photoresist over substrate 12) ; holographically patterning the photoresist layer to form a patterned mask (col. 38 line 60); transferring the pattern in the patterned mask into the solid state material by dry etching.(col. 26 line 64-65).

With respect to claim 2 Yoshimura describes the method of claim 1, wherein the photoresist comprises SU-8. (col.81 line 39)

With respect to claim 3 Yoshimura describes the method of claim 1, wherein said step of forming comprises spin coating the photoresist layer.(col. 75 line 52).

With respect to claim 4 Yoshimura describes the method of claim 1, wherein further comprising a step of, subsequent to said step of holographically patterning, optically direct writing a defect into the patterned mask. (col. 38 line 60, col. 62 lines 21-22, etc.).

Claim Rejections. 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 to 21 are rejected under 35 U.S.C. 103(a)as being unpatentable over

Yoshimura et al. (U.S. Patent No. 6,684,007, herein after Yoshimura) as applied to claims 1-4 above and further in view of Kumar et al. (U.S. Patent No. 5,223,356 herein after Kumar) also cite by applicant's in their IDS.

With respect to claim 5 Yoshimura describes the method of claim 4. Yoshimura does not specifically mention wherein said step of

holographically patterning comprises: conducting a first volumetric interfering of at least two beams.

However Kumar, a patent from the same field of endeavor describes in col. 11 lines 5 to 12 and col. 9 lines 65 to col. 10 line 7 describes conducting a first volumetric interfering of at least two beams, tomonitor and maintain desired diffraction efficiency of holographic image obtained by the two beams.

Therefore, it would have been obvious to one of ordinary skill in the art the time of the invention to include Kumar's step of holographically patterning comprises: conducting a first volumetric interfering of at least two beams in Yoshimura's method. The motivation to make the above combination is to monitor and maintain desired diffraction efficiency of holographic image obtained by the two beams (Kumar co1.11 lines 40-50).

The remaining limitations of claim 5 are :

and after changing the position of the solid state material and the photoresist layer, conducting a second volumetric interfering of at least two beams. (Kumar col. 11 lines 20-25).

With respect to claim 6 Yoshimura describes the method of claim 4, wherein said step of holographically patterning comprises changing the angle between two interfering beams used in the holographically patterning to introduce a period change in the periodic pattern.. (Kumar col. 11 lines 20-25).

With respect to claim 7 Yoshimura describes the method of claim 4, wherein said step of holographically patterning comprises changing the exposure time during the holographically patterning to introduce a duty cycle change in the periodic pattern.39 (Kumar fig. 6 -graph)

With respect to claim 8 Yoshimura describes the method of claim 4, further comprising steps of: post-exposure baking the photoresist layer exposed by said steps holographically patterning and optically direct writing; and developing the photoresist layer form the patterned mask. (Yoshimura col. 21 line 2-curing).

With respect to claim 9 Yoshimura describes the method of claim 8, comprising optimizing said steps holographically patterning and post-exposure baking to increase aspect ratios of the mask pattern transferred into the

photoresist layer and to increase the quality of the geometric shape of the mask pattern. (inherent to optimize the steps).

With respect to claims 10-14,16-17 Yoshimura describes. The method of claim 9, wherein optimizing said step of holographically patterning comprises adjusting exposure power per unit surface area, holographically patterning comprises determining an Optimal exposure time preliminary soft baking, performed immediately prior to said step of holographic patterning a sub-wavelength optical structure an optical grating having sub-wavelength spacing between grating elements. (Yoshimura examples and Kumar examples).

With respect to claim 15 Yoshimura describes the method of claim 8, wherein the exposure power in said step of holographic recording is in the range of 35 to 90mJ/cml. (Kumar col. 9 lines 40-45).

With respect to claims18 and 19 Yoshimura describes the method of claim 1, wherein the solid state material comprises a semiconductor quality Group III-V material layer (18) and GaAs (cl. 19) (Yoshimura col. 27 lines 30-35).

With respect to claim 20 Yoshimura describes a spectral filter, comprising: a substrate (12) ; a multi-layer structure having layers with alternating refractive indices (Yoshimura fig. 155-157, etc.); nanocavities etched into the multi-layer structure (Yoshimura fig.9 # 38) ; and periodic defects (34) in the multi-layer structure interrupting the alternating refractive indices with alternating periodically (periodic defects with alternating periods - well known in the art).

With respect to claim 21 Yoshimura describes a method for forming a photonic lattice pattern in a semi-conductor crystal: forming a photoresist layer on the semi-conductor crystal (col. 81 line 39 photoresist over substrate 12); exposing the photoresist layer by volumetric interference of at least two beams that create an interference pattern in the photoresist layer to expose a photonic lattice pattern (Kumar col. 11 lines 5 to 12 and col. 9 lines 65 to col. 10 line 7; creating at least one defect in the photonic lattice pattern by optical direct writing (well known in the art) : developing the photoresist layer to form a mask (Yoshimura col. 26 lines 1-20); and dry etching to pattern the semiconductor material and remove the mask. (Yoshimura col.26 lines 10-15).

Response to Arguments

Applicants; first contention that Yoshimura never discloses " patterning photoresist via holographic patterning and following the patterning by a dry etching" is not persuasive because as stated in the rejection above Yoshimura under summary of invention e.g. paras (d) etc. describes " Patterning" col.11 lines 4 to 10 describe " photoresist" and col. 38 line 60 etc. describe " holographic patterning" and col. 26 lines 1 to 15 describe dry etching after (i.e following) patterning and curing the photoresist .

Applicants' contention with respect to claim 4 that Yoshimura does not describe direct writing (of photodefects) into a hollographically formed mask is also not persuasive because as stated above Yoshimura teaches photodefects ina hollographically formed mask and (as stated in the rejection above col. 62 lines 21-22 describe use of writing beams , including SOLNET process i.e direct writing (of photodefects) into a hollographically formed mask.

Contrary to Applicants' contention Kumar descries a second patterning.

It is noted that that following response w.r.t claim 21 is also relevant to claim 20 namely the Visconti prior art discloses the well known in the art the nanocavities.

Applicants' contend with respect to claim 21 (page 4 of their remarks section) ," The examiner also asserts that the defect introduction in such a lattice pattern by optical direct lighting is well known in the art. Applicants know of no such well known practice, and invite the examiner to demonstrate that the writing of defects into a holographically patterned photoresist layer is well known in the art by citing art to support such a contention. :

The Examiner states for the record that the article entitled , " Nanopatterning Of Organic and In organic materials by holographic lithography and plasma etching " by P. Visconti et al. submitted by Applicants' in their IDS submitted 08/09/2007 is but

one example of such art that can support the examiner' s contention. A simple NPL search located at least six other articles.

Therefore all of applicants' arguments are not persuasive.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven H Rao/
Examiner, Art Unit 2814